

- c. Simplify $F = A \oplus B \oplus C + A$ to the simplest equivalent boolean expression and complete the truth table for F.
- d. Draw the CMOS implementation of an inverter (ie, NOT) using a pair of ideal transistors.
- e. Draw a FSM with the minimum states that, given a binary sequence as its inputs, outputs the remainder when the number of ones up to a point in the sequence is divided by 3. Draw the state table for this FSM.
- f. Draw a D-Latch using only basic logic gates.
- g. How many bits are needed in the address for a computer architecture with 2000 memory locations? What is stored at these addresses?
- h. Encode the instruction ADD, R1, R1, #2 to binary assuming that this instruction uses x86 encoding.
- i. Write a simple subroutine to find the difference of two numbers which are placed in R0 and R1 and stores the answer in R2. Assume that the numbers are stored in 2's complement. Use the LC-3 ISA provided to structure your instructions.
- j. Write a simple subroutine to sum the values of a null-terminated array (ie, the array is marked as complete in memory when a value of 0x0 is reached). Use the ARM ISA provided to structure your instructions. Hint: Use the BEQ loop statement.
- k. Describe, using the provided FSM for the data path of the LC3's interrupt sequence, how the LC3 ensures the proper operation of interrupted instructions, even when ISRs change condition bits.
- l. Given the following snippet of C code, predict the generated binary instructions of a compiler with high optimization and low optimization.